Topic:

Code Synthesis
Generating Code: Overview

We inductively generate instructions from the AST:
- there is a rule stating how to generate code for each non-terminal of the grammar
- the code is merely another attribute in the syntax tree
- code generation makes use of the already computed attributes
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In order to specify the code generation, we require

- a semantics of the language we are compiling (here: C standard)
- a semantics of the machine instructions
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- a semantics of the machine instructions

we commence by specifying machine instruction semantics
Chapter 1: The Register C-Machine
The Register C-Machine (R-CMa)

We generate Code for the Register C-Machine. The Register C-Machine is a virtual machine (VM).

- there exists no processor that can execute its instructions
- ... but we can build an interpreter for it
- we provide a visualization environment for the R-CMa
- the R-CMa has no `double`, `float`, `char`, `short` or `long` types
- the R-CMa has no instructions to communicate with the operating system
- the R-CMa has an unlimited supply of registers
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The R-CMa is more realistic than it may seem:

- the mentioned restrictions can easily be lifted
- the *Dalvik VM/ART* or the *LLVM* are similar to the R-CMa
- an interpreter of R-CMa can run on any platform
Virtual Machines

A virtual machine has the following ingredients:

- any virtual machine provides a set of instructions
- instructions are executed on virtual hardware
- the virtual hardware is a collection of data structures that is accessed and modified by the VM instructions
- ... and also by other components of the run-time system, namely functions that go beyond the instruction semantics
- the interpreter is part of the run-time system
Components of a Virtual Machine

Consider Java as an example:

A virtual machine such as the Dalvik VM has the following structure:

- **S**: the data store – a memory region in which cells can be stored in LIFO order (stack).
- **SP**: (stack pointer) pointer to the last used cell in S
- beyond S follows the memory containing the heap
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Consider Java as an example:

A virtual machine such as the Dalvik VM has the following structure:
- **S**: the data store – a memory region in which cells can be stored in LIFO order (stack).
- **SP**: (stack pointer) pointer to the last used cell in S.
- Beyond S follows the memory containing the heap.
- **C**: the memory storing code.
  - Each cell of C holds exactly one virtual instruction.
  - C can only be read.
- **PC**: (program counter) address of the instruction that is to be executed next.
  - PC contains 0 initially.
Executing a Program

- the machine loads an instruction from \( C[PC] \) into the instruction register \( IR \) in order to execute it
- before evaluating the instruction, the \( PC \) is incremented by one

\[
\text{while (true) \{ \\
IR = C[PC]; \quad PC++; \\
execute (IR); \\
\}}
\]

- node: the \( PC \) must be incremented before the execution, since an instruction may modify the \( PC \)
- the loop is exited by evaluating a \textit{halt} instruction that returns directly to the operating system
Chapter 2:
Generating Code for the Register C-Machine
Task: evaluate the expression \((1 + 7) \ast 3\)
that is, generate an instruction sequence that

- computes the value of the expression and
- keeps its value accessible in a reproducible way
Task: evaluate the expression \((1 + 7) \times 3\) that is, generate an instruction sequence that
- computes the value of the expression and
- keeps its value accessible in a reproducible way

Idea:
- first compute the value of the sub-expressions
- store the intermediate result in a temporary register
- apply the operator
- loop
Principles of the R-CMa

The R-CMa is composed of a stack, heap and a code segment, just like the JVM; it additionally has register sets:

- **local** registers are $R_1, R_2, \ldots R_i, \ldots$
- **global** register are $R_0, R_{-1}, \ldots R_j, \ldots$
The Register Sets of the R-CMa

The two register sets have the following purpose:

- **the local registers** $R_i$
  - save temporary results
  - store the contents of local variables of a function
  - can efficiently be stored and restored from the stack

Note: for now, we only use registers to store temporary computations

Idea for the translation: use a register counter $i$:
- registers $R_j$ with $j < i$ are in use
- registers $R_j$ with $j \geq i$ are available
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## Translation of Simple Expressions

Using variables stored in registers; loading constants:

<table>
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<tr>
<th>Instruction</th>
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<th>Intuition</th>
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<tbody>
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We define the following translation schema (with $\rho x = a$):

\[
\begin{align*}
\text{code}_R^i c \rho &= \text{loadc } R_i c \\
\text{code}_R^i x \rho &= \text{move } R_i R_a \\
\text{code}_R^i x = e \rho &= \text{code}_R^i e \rho \\
\text{move } &Ra Ri
\end{align*}
\]
Translation of Expressions

Let \( \text{op} = \{\text{add, sub, div, mul, mod, le, gr, eq, leq, geq, and, or}\} \). The R-CMa provides an instruction for each operator \( \text{op} \).

\[
\text{op} \ R_i \ R_j \ R_k
\]

where \( R_i \) is the target register, \( R_j \) the first and \( R_k \) the second argument.

Correspondingly, we generate code as follows:

\[
\text{code}_R^i \ e_1 \ \text{op} \ e_2 \ \rho = \begin{align*}
\text{code}_R^i \ e_1 \ \rho \\
\text{code}_R^{i+1} \ e_2 \ \rho \\
\text{op} \ R_i \ R_i \ R_{i+1}
\end{align*}
\]
Translation of Expressions

Let \( \text{op} = \{\text{add}, \text{sub}, \text{div}, \text{mul}, \text{mod}, \text{le}, \text{gr}, \text{eq}, \text{leq}, \text{geq}, \text{and}, \text{or}\} \). The R-CMa provides an instruction for each operator \( \text{op} \).

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\[
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\text{op} \ R_i \ R_i \ R_{i+1}
\end{cases}
\]

**Example:** Translate \( 3 \ast 4 \) with \( i = 4 \):

\[
\begin{align*}
\text{code}_R^4 \ 3 \ast 4 \ \rho & = \begin{cases} 
\text{code}_R^4 \ 3 \ \rho \\
\text{code}_R^5 \ 4 \ \rho \\
\text{mul} \ R_4 \ R_4 \ R_5
\end{cases}
\end{align*}
\]
Translation of Expressions

Let op = \{add, sub, div, mul, mod, le, gr, eq, leq, geq, and, or\}. The R-CMa provides an instruction for each operator op.

\[ \text{op } R_i \ R_j \ R_k \]

where \( R_i \) is the target register, \( R_j \) the first and \( R_k \) the second argument.

Correspondingly, we generate code as follows:

\[
\text{code}^i_{R} \ e_1 \ \text{op} \ e_2 \ \rho \quad = \quad \begin{align*}
\text{code}^i_{R} \ e_1 \ \rho \\
\text{code}^{i+1}_{R} \ e_2 \ \rho \\
\text{op} \ R_i \ R_i \ R_{i+1}
\end{align*}
\]

Example: Translate \(3 \times 4\) with \(i = 4\):

\[
\text{code}^{4}_{R} \ 3 \times 4 \ \rho \quad = \quad \begin{align*}
\text{loadc} \ R_4 \ 3 \\
\text{loadc} \ R_5 \ 4 \\
\text{mul} \ R_4 \ R_4 \ R_5
\end{align*}
\]
Managing Temporary Registers

Observe that temporary registers are re-used: translate $3 \times 4 + 3 \times 4$ with $t = 4$:

$$\text{code}_R^4 \ 3 \times 4 + 3 \times 4 \ \rho \ = \ \text{code}_R^4 \ 3 \times 4 \ \rho$$

$$\text{code}_R^5 \ 3 \times 4 \ \rho \ = \ \text{add} \ R_4 \ R_4 \ R_5$$

where

$$\text{code}_R^i \ 3 \times 4 \ \rho \ = \ \text{loadc} \ R_i \ 3$$

$$\text{loadc} \ R_{i+1} \ 4$$

$$\text{mul} \ R_i \ R_i \ R_{i+1}$$

we obtain

$$\text{code}_R^4 \ 3 \times 4 + 3 \times 4 \ \rho \ = \$$
Managing Temporary Registers

Observe that temporary registers are re-used: translate $3 \times 4 + 3 \times 4$ with $t = 4$:

$$
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$$

$$
\text{add} \ R_4 \ R_4 \ R_5
$$

where

$$
\text{code}_R^i \ 3 \times 4 \ \rho \ = \ \text{loadc} \ R_i \ 3
$$

$$
\text{loadc} \ R_{i+1} \ 4
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$$
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$$

we obtain

$$
\text{code}_R^4 \ 3 \times 4 + 3 \times 4 \ \rho \ = \ \text{loadc} \ R_4 \ 3
$$

$$
\text{loadc} \ R_5 \ 4
$$

$$
\text{mul} \ R_4 \ R_4 \ R_5
$$

$$
\text{loadc} \ R_5 \ 3
$$

$$
\text{loadc} \ R_6 \ 4
$$

$$
\text{mul} \ R_5 \ R_5 \ R_6
$$

$$
\text{add} \ R_4 \ R_4 \ R_5
$$
Semantics of Operators

The operators have the following semantics:

- **add** $R_i \ R_j \ R_k \quad R_i = R_j + R_k$
- **sub** $R_i \ R_j \ R_k \quad R_i = R_j - R_k$
- **div** $R_i \ R_j \ R_k \quad R_i = R_j / R_k$
- **mul** $R_i \ R_j \ R_k \quad R_i = R_j \cdot R_k$
- **mod** $R_i \ R_j \ R_k \quad R_i = \text{signum}(R_k) \cdot k \quad \text{with} \quad |R_j| = n \cdot |R_k| + k \land n \geq 0, 0 \leq k < |R_k|$
- **le** $R_i \ R_j \ R_k \quad R_i = \text{if } R_j < R_k \text{ then } 1 \text{ else } 0$
- **gr** $R_i \ R_j \ R_k \quad R_i = \text{if } R_j > R_k \text{ then } 1 \text{ else } 0$
- **eq** $R_i \ R_j \ R_k \quad R_i = \text{if } R_j = R_k \text{ then } 1 \text{ else } 0$
- **leq** $R_i \ R_j \ R_k \quad R_i = \text{if } R_j \leq R_k \text{ then } 1 \text{ else } 0$
- **geq** $R_i \ R_j \ R_k \quad R_i = \text{if } R_j \geq R_k \text{ then } 1 \text{ else } 0$
- **and** $R_i \ R_j \ R_k \quad R_i = R_j \ & \ R_k \quad \text{ // bit-wise and}$
- **or** $R_i \ R_j \ R_k \quad R_i = R_j \ | \ R_k \quad \text{ // bit-wise or}$

Note: all registers and memory cells contain operands in $\mathbb{Z}_{15} / 49$
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- **div** $R_i \ R_j \ R_k \quad R_i = R_j / R_k$
- **mul** $R_i \ R_j \ R_k \quad R_i = R_j \ast R_k$
- **mod** $R_i \ R_j \ R_k \quad R_i = \text{signum}(R_k) \cdot k$ with $|R_j| = n \cdot |R_k| + k \wedge n \geq 0, 0 \leq k < |R_k|$
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Note: all registers and memory cells contain operands in $\mathbb{Z}$
Translation of Unary Operators

Unary operators $\mathit{op} = \{\mathit{neg}, \mathit{not}\}$ take only two registers:

$$\text{code}_R^i \ \mathit{op} \ e \ \rho = \begin{cases} \text{code}_R^i \ e \ \rho \\ \mathit{op} \ R_i \ R_i \end{cases}$$
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$$\begin{align*}
\text{code}_R^i \text{ op } e \rho & = \text{code}_R^i e \rho \\
\text{op } R_i R_i
\end{align*}$$

Note: We use the same register.
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\ \text{op} \ R_i \ R_i
\]

Note: We use the same register.

Example: Translate \(-4\) into \(R_5\):

\[
\text{code}_R^5 \ -4 \ \rho = \ \text{code}_R^5 \ 4 \ \rho \\
\neg \ R_5 \ R_5
\]
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Unary operators $\text{op} = \{\text{neg, not}\}$ take only two registers:

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Example: Translate $-4$ into $R_5$:

$$\text{code}_R^5 -4 \rho = \text{loadc } R_5 4$$

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The operators have the following semantics:

$$\begin{align*}
\text{not} \ R_i \ R_j & \quad R_i \leftarrow \text{if } R_j = 0 \text{ then } 1 \text{ else } 0 \\
\text{neg} \ R_i \ R_j & \quad R_i \leftarrow -R_j
\end{align*}$$
Applying Translation Schema for Expressions

Suppose the following function is given:

```c
void f(void) {
    int x, y, z;
    x = y + z * 3;
}
```

- Let \( \rho = \{x \mapsto 1, y \mapsto 2, z \mapsto 3\} \) be the address environment.
- Let \( R_4 \) be the first free register, that is, \( i = 4 \).

\[
\begin{align*}
\text{code}^4_{x} &= \text{y}+\text{z} \ast 3 \quad \rho \\
\text{move} R_1 R_4
\end{align*}
\]
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Let \( R_4 \) be the first free register, that is, \( i = 4 \).

- \( \text{code}^4_{R} \quad x = y + z * 3 \quad \rho = \text{code}^4_{R} \quad y + z * 3 \quad \rho \)
- \( \text{move} \quad R_1 \quad R_4 \)
- \( \text{code}^5_{R} \quad y + z * 3 \quad \rho = \text{move} \quad R_4 \quad R_2 \)
- \( \text{code}^5_{R} \quad z * 3 \quad \rho \)
- \( \text{add} \quad R_4 \quad R_4 \quad R_5 \)
- \( \text{code}^5_{R} \quad z * 3 \quad \rho = \text{move} \quad R_5 \quad R_3 \)
- \( \text{code}^6_{R} \quad 3 \quad \rho \)
- \( \text{mul} \quad R_5 \quad R_5 \quad R_6 \)
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\[
\begin{align*}
\text{code}^4 & \quad x = y + z * 3 \quad \rho = \quad \text{code}_R^4 \quad y + z * 3 \quad \rho \\
& \quad \quad \text{move} \quad R_1 \quad R_4 \\
\text{code}_R^4 & \quad y + z * 3 \quad \rho = \quad \text{move} \quad R_4 \quad R_2 \\
& \quad \quad \text{code}_R^5 \quad z * 3 \quad \rho \\
& \quad \quad \text{add} \quad R_4 \quad R_4 \quad R_5 \\
\text{code}_R^5 & \quad z * 3 \quad \rho = \quad \text{move} \quad R_5 \quad R_3 \\
& \quad \quad \text{code}_R^6 \quad 3 \quad \rho \\
& \quad \quad \text{mul} \quad R_5 \quad R_5 \quad R_6 \\
\text{code}_R^6 & \quad 3 \quad \rho = \quad \text{loadc} \quad R_6 \quad 3
\end{align*}
\]
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Let \( R_4 \) be the first free register, that is, \( i = 4 \).

\[
\begin{align*}
\text{code}^4_{\rho} x & = y + z \cdot 3 & \text{move} & R_1 R_4 \\
\text{code}^4_{\rho} y & + z \cdot 3 & \text{move} & R_4 R_2 \\
\text{code}^5_{\rho} z \cdot 3 & \text{add} & R_4 R_4 R_5 \\
\text{code}^6_{\rho} 3 & \text{mul} & R_5 R_5 R_6 \\
\text{loadc} & R_6 3
\end{align*}
\]

\( \rightarrow \) the assignment \( x = y + z \cdot 3 \) is translated as

\[
\begin{align*}
\text{move} & \ R_4 R_2; \text{move} \ R_5 R_3; \text{loadc} \ R_6 3; \text{mul} \ R_5 R_5 R_6; \text{add} \ R_4 R_4 R_5; \text{move} \ R_1 R_4
\end{align*}
\]
Chapter 3:
Statements and Control Structures
About Statements and Expressions

General idea for translation:

\[
\begin{align*}
\text{code}^i s \rho & \quad : \quad \text{generate code for statement } s \\
\text{code}^i_R e \rho & \quad : \quad \text{generate code for expression } e \text{ into } R_i
\end{align*}
\]

Throughout: \( i, i + 1, \ldots \) are free (unused) registers
About Statements and Expressions

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\]

Throughout: \( i, i + 1, \ldots \) are free (unused) registers

For an \textit{expression} \( x = e \) with \( \rho x = a \) we defined:

\[
\text{code}^i_R x = e \rho = \text{code}^i_R e \rho
\]

\[
\text{move } R_a R_i
\]

However, \( x = e; \) is also an \textit{expression statement}:
About Statements and Expressions

General idea for translation:
\[
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For an expression \( x = e \) with \( \rho x = a \) we defined:
\[
\text{code}^i_R x = e \rho \quad = \quad \text{code}^i e \rho
\]
move \( R_a R_i \)

However, \( x = e \); is also an expression statement:

- Define:
\[
\text{code}^i e_1 = e_2; \ \rho \quad = \quad \text{code}^i_R e_1 = e_2 \ \rho
\]

The temporary register \( R_i \) is ignored here. More general:
\[
\text{code}^i e; \ \rho = \text{code}^i_R e \ \rho
\]
About Statements and Expressions

General idea for translation:

- \( \text{code}^i s \rho \) : generate code for statement \( s \)
- \( \text{code}^i_R e \rho \) : generate code for expression \( e \) into \( R_i \)

Throughout: \( i, i+1, \ldots \) are free (unused) registers

For an expression \( x = e \) with \( \rho x = a \) we defined:

\[
\text{code}^i_R x = e \rho = \text{code}^i_R e \rho \\
\text{move } R_a \rightarrow R_i
\]

However, \( x = e; \) is also an expression statement:

- Define:

\[
\text{code}^i e_1 = e_2; \rho = \text{code}^i_R e_1 = e_2 \rho
\]

The temporary register \( R_i \) is ignored here. More general:

\[
\text{code}^i e; \rho = \text{code}^i_R e \rho
\]

- Observation: the assignment to \( e_1 \) is a side effect of the evaluating the expression \( e_1 = e_2 \).
The code for a sequence of statements is the concatenation of the instructions for each statement in that sequence:

\[
\text{code}^i (s \; ss) \; \rho = \text{code}^i s \; \rho \\
\text{code}^i ss \; \rho \\
\text{code}^i \varepsilon \; \rho = // \text{ empty sequence of instructions}
\]

Note here: \( s \) is a statement, \( ss \) is a sequence of statements
In order to diverge from the linear sequence of execution, we need jumps:

\[ PC = A; \]
A conditional jump branches depending on the value in $R_i$:

- If $R_i \neq 0$, execute code at address $A$.
- If $R_i = 0$, continue execution at the current program counter.

$$\text{if } (R_i == 0) \text{ PC }= A;$$
Simple Conditional

We first consider $s \equiv \textbf{if} (c) \textbf{ ss}$.  
...and present a translation without basic blocks.

Idea:
- emit the code of $c$ and $ss$ in sequence
- insert a jump instruction in-between, so that correct control flow is ensured

$$
\begin{align*}
\text{code}^i s \rho &= \text{code}^i R c \rho \\
&\quad \text{jumpz} R_i A \\
\text{code}^i ss \rho \\
A : &\ldots
\end{align*}
$$
Translation of $\text{if (c) tt else ee}$.

$$\text{code}^i \ \text{if(c) tt else ee } \rho = $$

$$\begin{align*}
\text{code}^i & \ c \ \rho \\
\text{jumpz} & \\
\text{jumpz} & \ R_i \ A \\
\text{code}^i & \ tt \ \rho \\
\text{jump} & \\
A : & \ \text{code}^i \ ee \ \rho \\
B : & \\
\end{align*}$$
Example for if-statement

Let $\rho = \{x \mapsto 4, y \mapsto 7\}$ and let $s$ be the statement

```plaintext
if (x>y) {
   /* (i) */
   x = x - y;
   /* (ii) */
}
else {
   y = y - x;
   /* (iii) */
}
```

Then code $^i s \rho$ yields:
Example for if-statement

Let $\rho = \{x \mapsto 4, y \mapsto 7\}$ and let $s$ be the statement

```java
if (x>y) {
   /* (i) */
   x = x - y;
   /* (ii) */
} else {
   y = y - x;
   /* (iii) */
}
```

Then code $s$ $\rho$ yields:

(i) move $R_i R_4$
move $R_{i+1} R_7$
gr $R_i R_i R_{i+1}$
nmpz $R_i A$

(ii) move $R_i R_4$
move $R_{i+1} R_7$
sub $R_i R_i R_{i+1}$
mov $R_4 R_i$
njump $B$

(iii) move $R_i R_7$
move $R_{i+1} R_4$
sub $R_i R_i R_{i+1}$
mov $R_7 R_i$
njump $B$
We only consider the loop \( s \equiv \textbf{while} (e) \ s' \). For this statement we define:

\[
\text{code}^i \textbf{while}(e) \ s \ \rho \ = \ A : \ \text{code}^i_{R} \ e \ \rho \\
\text{jumpz} \ R_i \ B \\
\text{code}^i \ s \ \rho \\
\text{jump} \ A \\
B : \\
\text{code}_R \text{ for } e
\]
Example: Translation of Loops

Let $\rho = \{ a \mapsto 7, b \mapsto 8, c \mapsto 9 \}$ and let $s$ be the statement:

```c
while (a>0) {
    c = c + 1; /* (i) */
    a = a - b; /* (ii) */
}
```

Then $\text{code}^i s \rho$ evaluates to:
Example: Translation of Loops

Let $\rho = \{a \mapsto 7, b \mapsto 8, c \mapsto 9\}$ and let $s$ be the statement:

```c
while (a>0) {
    c = c + 1; /* (i) */
    a = a - b; /* (ii) */
}
```

Then code $s \rho$ evaluates to:

(i) $A$:
- move $R_i R_7$
- loadc $R_{i+1} 0$
- gr $R_i R_i R_{i+1}$
- jumpz $R_i B$

(ii) $B$:
- move $R_i R_9$
- loadc $R_{i+1} 1$
- add $R_i R_i R_{i+1}$

(iii) $C$:
- move $R_i R_7$
- move $R_i R_8$
- sub $R_i R_i R_{i+1}$
- move $R_7 R_i$
- jump $A$
for-Loops

The for-loop $s \equiv \textbf{for} \ (e_1; e_2; e_3) \ s'$ is equivalent to the statement sequence $e_1; \ \textbf{while} \ (e_2) \ \{s' \ e_3;\} –$ as long as $s'$ does not contain a \textbf{continue} statement.

Thus, we translate:

$$\text{code}^i \ \textbf{for}(e_1; e_2; e_3) \ s \ \rho \ = \ \text{code}^i_\mathcal{R} \ e_1 \ \rho$$

$$A:\ \text{code}^i_\mathcal{R} \ e_2 \ \rho$$

$$\text{jumpz} \ R_i \ B$$

$$\text{code}^i \ s \ \rho$$

$$\text{code}^i_\mathcal{R} \ e_3 \ \rho$$

$$\text{jump} \ A$$

$$B:\$$
The switch-Statement

Idea:

- Suppose choosing from multiple options in *constant time* if possible
- use a *jump table* that, at the $i$th position, holds a jump to the $i$th alternative
- in order to realize this idea, we need an *indirect jump* instruction
The switch-Statement

Idea:
- Suppose choosing from multiple options in \textit{constant time} if possible
- use a \textit{jump table} that, at the \textit{i}th position, holds a jump to the \textit{i}th alternative
- in order to realize this idea, we need an \textit{indirect jump} instruction

\[
PC = A + R_i;
\]
Consecutive Alternatives

Let `switch` $s$ be given with $k$ consecutive `case` alternatives:

```java
switch (e) {
    case 0:  $s_0$; break;
    // ...
    case $k-1$:  $s_{k-1}$; break;
    default:  $s_k$; break;
}
```
Consecutive Alternatives

Let `switch s` be given with `k` consecutive `case` alternatives:

```java
switch (e) {
    case 0: s0; break;
    :
    case k - 1: sk-1; break;
    default: sk; break;
}
```

Define `code^i s ρ` as follows:

- `code^i s ρ = code^i e ρ`
- `check^i 0 k B`
- `A0 : code^i s0 ρ`
- `jump C`
- `Ak : code^i sk ρ`
- `jump C`
- `B : jump A0`
- `C :`
Consecutive Alternatives

Let `switch`\(s\) be given with \(k\) consecutive `case` alternatives:

```java
switch (e) {
    case 0: s0; break;
    :
    case k - 1: sk-1; break;
    default: sk; break;
}
```

Define `code^i s \rho` as follows:

- `code^i s \rho = code^i R e \rho`
- `check^i 0 k B B : jump A_0`
- `A_0 : code^i s_0 \rho : :`
- `jump C jump A_k`
- `C :`
- `A_k : code^i s_k \rho`
- `jump C`

`check^i l u B` checks if \(l \leq R_i < u\) holds and jumps accordingly.
Translation of the \texttt{check}^i Macro

The macro \texttt{check}^i \ l \ u \ B checks if \( l \leq R_i < u \). Let \( k = u - l \).

- if \( l \leq R_i < u \) it jumps to \( B + R_i - l \)
- if \( R_i < l \) or \( R_i \geq u \) it jumps to \( A_k \)

\[
\begin{align*}
B : & \quad \text{jump } A_0 \\
: & \quad : \\
: & \quad \text{jump } A_k \\
C : & 
\end{align*}
\]
Translation of the \( \text{check}^i \) Macro

The macro \( \text{check}^i \ l \ u \ B \) checks if \( l \leq R_i < u \). Let \( k = u - l \).

- if \( l \leq R_i < u \) it jumps to \( B + R_i - l \)
- if \( R_i < l \) or \( R_i \geq u \) it jumps to \( A_k \)

we define:

\[
\text{check}^i \ l \ u \ B = \begin{array}{l}
\text{loadc } R_{i+1} \ l \\
\text{geq } R_{i+2} \ R_i \ R_{i+1} \\
\text{jumpz } R_{i+2} \ E \\
\text{sub } R_i \ R_i \ R_{i+1} \\
\text{loadc } R_{i+1} \ k \\
\text{geq } R_{i+2} \ R_i \ R_{i+1} \\
\text{jumpz } R_{i+2} \ D \\
\text{loadc } R_i \ k \\
\text{jumpi } R_i \ B
\end{array}
\]

\[
\begin{align*}
B : & \text{ jump } A_0 \\
E : & \text{ loadc } R_i \ k \\
D : & \text{ jumpi } R_i \ B \\
C : & \text{ jump } A_k
\end{align*}
\]
Translation of the $check^i$ Macro

The macro $check^i l u B$ checks if $l \leq R_i < u$. Let $k = u - l$.

- if $l \leq R_i < u$ it jumps to $B + R_i - l$
- if $R_i < l$ or $R_i \geq u$ it jumps to $A_k$

we define:

$$check^i l u B = \begin{array}{l}
\text{loadc } R_{i+1} l \\
\text{geq } R_{i+2} R_i R_{i+1} \\
\text{jumpz } R_{i+2} E \\
\text{sub } R_i R_i R_{i+1} \\
\text{loadc } R_{i+1} k \\
\text{geq } R_{i+2} R_i R_{i+1} \\
\text{jumpz } R_{i+2} D \\
\text{jumpi } R_i B \\
\text{jump A}_0 \end{array}$$

Note: a jump $\text{jumi} R_i B$ with $R_i = u$ winds up at $B + u$, the default case
This translation is only suitable for *certain* switch-statement.

- In case the table starts with 0 instead of $u$ we don’t need to subtract it from $e$ before we use it as index

- if the value of $e$ is guaranteed to be in the interval $[l, u]$, we can omit check
General translation of switch-Statements

In general, the values of the various cases may be far apart:

- generate an if-ladder, that is, a sequence of if-statements
- for $n$ cases, an if-cascade (tree of conditionals) can be generated $\sim O(\log n)$ tests
- if the sequence of numbers has small gaps ($\leq 3$), a jump table may be smaller and faster
- one could generate several jump tables, one for each sets of consecutive cases
- an if cascade can be re-arranged by using information from profiling, so that paths executed more frequently require fewer tests
Chapter 4:
Functions
Ingredients of a Function

The definition of a function consists of

- a name with which it can be called;
- a specification of its formal parameters;
- possibly a result type;
- a sequence of statements.

In C we have:

\[
\text{code}^i_R f \rho = \text{loadc } R_i \_f \text{ with } \_f \text{ starting address of } f
\]

Observe:

- function names must have an address assigned to them
- since the size of functions is unknown before they are translated, the addresses of forward-declared functions must be inserted later
Memory Management in Functions

```c
int fac(int x) {
    if (x<=0) return 1;
    else return x*fac(x-1);
}
```

```c
int main(void) {
    int n;
    n = fac(2) + fac(1);
    printf("%d", n);
}
```

At run-time several instances may be active, that is, the function has been called but has not yet returned.

The recursion tree in the example:
Memory Management in Function Variables

The formal parameters and the local variables of the various instances of a function must be kept separate.

Idea for implementing functions:

- set up a region of memory each time it is called
- in sequential programs this memory region can be allocated on the stack
- thus, each instance of a function has its own region on the stack
- these regions are called stack frames
Organization of a Stack Frame

- stack representation: grows upwards
- SP points to the last used stack cell

![Stack Frame Diagram]

- local memory
callee

- organizational
cells
Organization of a Stack Frame

- **stack** representation: grows upwards
- **SP** points to the last used stack cell

**FP** = frame pointer: points to the last organizational cell
- used to recover the previously active stack frame
Split of Obligations

Definition

Let $f$ be the current function that calls a function $g$.

- $f$ is dubbed *caller*
- $g$ is dubbed *callee*

The code for managing function calls has to be split between caller and callee. This split cannot be done arbitrarily since some information is only known in that caller or only in the callee.

Observation:

The space requirement for parameters is only know by the caller:

Example: `printf`
Principle of Function Call and Return

actions taken on entering $g$:

1. compute the start address of $g$
2. compute actual parameters in globals
3. backup of caller-save registers
4. backup of FP
5. set the new FP
6. back up of PC and jump to the beginning of $g$
7. copy actual params to locals

actions taken on leaving $g$:

1. compute the result into $R_0$
2. restore FP, SP
3. return to the call site in $f$, that is, restore PC
4. restore the caller-save registers

} saveloc
\{ mark \} are in $f$
\} call
\{ ... \} is in $g$

} return \} are in $g$
\} restoreloc \} is in $f$
Managing Registers during Function Calls

The two register sets (global and local) are used as follows:

- automatic variables live in *local* registers $R_i$
- intermediate results also live in *local* registers $R_i$
- parameters live in *global* registers $R_i$ (with $i \leq 0$)
- global variables:
Managing Registers during Function Calls

The two register sets (global and local) are used as follows:

- automatic variables live in \textit{local} registers $R_i$
- intermediate results also live in \textit{local} registers $R_i$
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- global variables: let’s suppose there are none

convention:
Managing Registers during Function Calls

The two register sets (global and local) are used as follows:

- automatic variables live in *local* registers $R_i$
- intermediate results also live in *local* registers $R_i$
- parameters live in *global* registers $R_i$ (with $i \leq 0$)
- global variables: let's suppose there are none

convention:

- the $i$th argument of a function is passed in register $R_{-i}$
- the result of a function is stored in $R_0$
- local registers are saved before calling a function
Managing Registers during Function Calls

The two register sets (global and local) are used as follows:

- automatic variables live in \textit{local} registers $R_i$
- intermediate results also live in \textit{local} registers $R_i$
- parameters live in \textit{global} registers $R_i$ (with $i \leq 0$)
- global variables: let’s suppose there are none

convention:

- the $i$th argument of a function is passed in register $R_{-i}$
- the result of a function is stored in $R_0$
- local registers are saved before calling a function

Definition

Let $f$ be a function that calls $g$. A register $R_i$ is called

- \textit{caller-saved} if $f$ backs up $R_i$ and $g$ may overwrite it
- \textit{callee-saved} if $f$ does not back up $R_i$, and $g$ must restore it before returning
Translation of Function Calls

A function call $g(e_1, \ldots, e_n)$ is translated as follows:

$$\text{code}_R^i \ g(e_1, \ldots, e_n) \rho = \text{code}_R^i \ g \rho$$

$$\text{code}_R^{i+1} \ e_1 \rho$$

$$\vdots$$

$$\text{code}_R^{i+n} \ e_n \rho$$

move $R_{i-1} \ R_{i+1}$

$$\vdots$$

move $R_{i-n} \ R_{i+n}$

saveloc $R_1 \ R_{i-1}$

mark

call $R_i$

restoreloc $R_1 \ R_{i-1}$

move $R_i \ R_0$
Translation of Function Calls

A function call \( g(e_1, \ldots e_n) \) is translated as follows:

\[
\begin{align*}
\text{code}_{R}^{i} g(e_1, \ldots e_n) & \quad \rho = \text{code}_{R}^{i} g \quad \rho \\
\text{code}_{R}^{i+1} e_1 & \quad \rho \\
\vdots \\
\text{code}_{R}^{i+n} e_n & \quad \rho \\
\text{move} & \quad R_{i-1} \; R_{i+1} \\
\vdots \\
\text{move} & \quad R_{i-n} \; R_{i+n} \\
\text{saveloc} & \quad R_1 \; R_{i-1} \\
\text{mark} \\
\text{call} & \quad R_i \\
\text{restoreloc} & \quad R_1 \; R_{i-1} \\
\text{move} & \quad R_i \; R_0
\end{align*}
\]

New instructions:

- \text{saveloc} \( R_i \; R_j \) pushes the registers \( R_i, R_{i+1}, \ldots R_j \) onto the stack
- \text{mark} backs up the organizational cells
- \text{call} \( R_i \) calls the function at the address in \( R_i \)
- \text{restoreloc} \( R_i \; R_j \) pops \( R_j, R_{j-1}, \ldots R_i \) off the stack
Rescuing the FP

The instruction **mark** allocates stack space for the return value and the organizational cells and backs up FP.

\[
\text{S[SP+1] = FP;}
\]
\[
\text{SP = SP + 1;}
\]
Calling a Function

The instruction call rescues the value of PC+1 onto the stack and sets FP and PC.

\[
\begin{align*}
\text{call Ri} & \\
\text{FP} & = \text{SP} \\
\text{PC} & = \text{Ri} \\
\end{align*}
\]

\[
\begin{align*}
\text{SP} & = \text{SP} + 1; \\
\text{S}[\text{SP}] & = \text{PC}; \\
\text{FP} & = \text{SP}; \\
\text{PC} & = \text{Ri};
\end{align*}
\]
The global register set is also used to communicate the result value of a function:

\[
\text{code}_i \text{ return } e \rho = \text{code}_R e \rho
\]

move \( R_0 \) \( R_i \)

return
The global register set is also used to communicate the result value of a function:

\[
\begin{align*}
\text{code}^i \text{return } e &\rho \quad = \\
\text{code}_R^i \ e &\rho \\
\text{move } R_0 &\ R_i \\
\text{return }
\end{align*}
\]

alternative without result value:

\[
\begin{align*}
\text{code}^i \text{return } &\rho \quad = \\
\text{return }
\end{align*}
\]
The global register set is also used to communicate the result value of a function:

\[
\text{code}^i \ \text{return} \ e \ \rho \ = \ \text{code}^R_\text{R} \ e \ \rho \\
\text{move} \ R_0 \ R_i \\
\text{return}
\]

alternative without result value:

\[
\text{code}^i \ \text{return} \ \rho \ = \ \text{return}
\]

*global* registers are otherwise not used inside a function body:

- **advantage:** at any point in the body another function can be called without backing up *global* registers
- **disadvantage:** on entering a function, all *global* registers must be saved
Return from a Function

The instruction return relinquishes control of the current stack frame, that is, it restores PC and FP.

\[
\begin{align*}
\text{PC} &= S[\text{FP}] ; \\
\text{SP} &= \text{FP}-2 ; \\
\text{FP} &= S[\text{SP}+1] ;
\end{align*}
\]
Translation of Functions

The translation of a function is thus defined as follows:

$$\mathrm{code}^1 \ t_r \ f(\text{args})\{\text{decls} \ ss\} \ \rho \ = \ \begin{array}{l}
\text{move} \ R_{l+1} \ R_{-1} \\
\vdots \\
\text{move} \ R_{l+n} \ R_{-n} \\
\text{code}^{l+n+1} \ ss \ \rho' \\
\text{return}
\end{array}$$

Assumptions:

- the function has $n$ parameters
- the local variables are stored in registers $R_1,...,R_l$
- the parameters of the function are in $R_{-1},...,R_{-n}$
- $\rho'$ is obtained by extending $\rho$ with the bindings in decls and the function parameters
- return is not always necessary

Are the move instructions always necessary?
Translation of Functions

The translation of a function is thus defined as follows:

\[
\text{code}^1 \ t_r \ f(args)\{decls \ ss\} \ \rho \ = \ \begin{array}{l}
\text{move} \ R_{l+1} \ R_{-1} \\
\vdots \\
\text{move} \ R_{l+n} \ R_{-n} \\
\text{code}^{l+n+1} \ ss \ \rho' \\
\text{return}
\end{array}
\]

Assumptions:

- the function has \( n \) parameters
The translation of a function is thus defined as follows:

\[
\text{code}^1 \ t_r \ f(\text{args})\{\text{decls} \ ss\} \ \rho = \text{move } R_{l+1} R_{-1} \\
\vdots \\
\text{move } R_{l+n} R_{-n} \\
\text{code}^{l+n+1} \ ss \ \rho' \\
\text{return}
\]

Assumptions:
- the function has \( n \) parameters
- the local variables are stored in registers \( R_1, \ldots R_l \)
The translation of a function is thus defined as follows:

\[
\text{code}^1 \ t_r \ f(\text{args})\{\text{decls} \ ss\} \ \rho = \ \text{move} \ R_{l+1} \ R_{-1} \\
\vdots \\
\text{move} \ R_{l+n} \ R_{-n} \\
\text{code}^{l+n+1} \ ss \ \rho' \\
\text{return}
\]

Assumptions:
- the function has \( n \) parameters
- the local variables are stored in registers \( R_1, \ldots R_l \)
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Translation of Functions

The translation of a function is thus defined as follows:

\[
\text{code}^1 \ t_r \ f(\text{args})\{\text{decls} \ ss\} \ \rho = \ \text{move} \ R_{l+1} \ R_{-1} \\
\quad \vdots \\
\quad \text{move} \ R_{l+n} \ R_{-n} \\
\text{code}^{l+n+1} \ ss \ \rho' \\
\text{return}
\]

Assumptions:
- the function has \( n \) parameters
- the local variables are stored in registers \( R_1, \ldots, R_l \)
- the parameters of the function are in \( R_{-1}, \ldots, R_{-n} \)
- \( \rho' \) is obtained by extending \( \rho \) with the bindings in \( \text{decls} \) and the function parameters \( \text{args} \)
Translation of Functions

The translation of a function is thus defined as follows:

\[
\text{code}^1 \ t_r \ f(\text{args})\{\text{decls} \ ss\} \ \rho \ = \ \begin{array}{l}
\text{move} \ R_{l+1} \ R_{-1} \\
\vdots \\
\text{move} \ R_{l+n} \ R_{-n} \\
\text{code}^{l+n+1} \ ss \ \rho' \\
\text{return}
\end{array}
\]

Assumptions:
- the function has \( n \) parameters
- the local variables are stored in registers \( R_1, \ldots, R_l \)
- the parameters of the function are in \( R_{-1}, \ldots, R_{-n} \)
- \( \rho' \) is obtained by extending \( \rho \) with the bindings in \( \text{decls} \) and the function parameters \( \text{args} \)
- return is not always necessary
Translation of Functions

The translation of a function is thus defined as follows:

\[
\text{code}^1 \ t_r \ f(\text{args}) \{ \text{decls} \ ss \} \ \rho \ = \ \begin{align*}
&\text{move } R_{l+1} \ R_{-1} \\
&\vdots \\
&\text{move } R_{l+n} \ R_{-n} \\
&\text{code}^{l+n+1} \ ss \ \rho' \\
&\text{return}
\end{align*}
\]

Assumptions:

- the function has \( n \) parameters
- the local variables are stored in registers \( R_1, \ldots, R_l \)
- the parameters of the function are in \( R_{-1}, \ldots, R_{-n} \)
- \( \rho' \) is obtained by extending \( \rho \) with the bindings in \( \text{decls} \) and the function parameters \( \text{args} \)
- return is not always necessary

Are the move instructions always necessary?
Translation of Whole Programs

A program \( P = F_1; \ldots F_n \) must have a single main function.

\[
\text{code}^1 P \rho = \text{loadc } R_1 \_\text{main}
\]
\[\text{mark} \]
\[\text{call } R_1 \]
\[\text{halt} \]
\[\_f_1 : \text{code}^1 F_1 \rho \oplus \rho_{f_1} \]
\[\vdots \]
\[\_f_n : \text{code}^1 F_n \rho \oplus \rho_{f_n} \]

Assumptions:
\( \rho = \emptyset \) assuming that we have no global variables
\( \rho_{f_i} \) contain the addresses of the functions up to \( f_i \)
\( \rho_1 \oplus \rho_2 = \lambda x. \begin{cases} \rho_2(x) & \text{if } x \in \text{dom}(\rho_2) \\ \rho_1(x) & \text{otherwise} \end{cases} \)
Translation of Whole Programs

A program \( P = F_1; \ldots F_n \) must have a single main function.

\[
\text{code}^1 \ P \ \rho = \ \text{loadc} \ R_1 \ _\text{main} \\
\text{mark} \\
\text{call} \ R_1 \\
\text{halt} \\
\_f_1 : \ \text{code}^1 \ F_1 \ \rho \oplus \ \rho_{f_1} \\
\vdots \\
\_f_n : \ \text{code}^1 \ F_n \ \rho \oplus \ \rho_{f_n}
\]

Assumptions:

- \( \rho = \emptyset \) assuming that we have no global variables
- \( \rho_{f_i} \) contain the addresses of the functions up to \( f_i \)
- \( \rho_1 \oplus \rho_2 = \lambda x . \begin{cases} \rho_2(x) & \text{if } x \in \text{dom}(\rho_2) \\ \rho_1(x) & \text{otherwise} \end{cases} \)
Translation of the \texttt{fac}-function

Consider:

\begin{verbatim}
int fac(int x) {
    if (x<=0)
        return 1;
    else
        return x*fac(x-1);
}
\end{verbatim}

\begin{verbatim}
\_fac:  move R1 R1   save param.
i = 2  move R2 R1   if (x<=0)
loadc R3 0
leq R2 R2 R3
jumpz R2 \_A  to else
loadc R2 1
return
jump \_B  code is dead

\_A:  move R2 R1   x*fac(x-1)
i = 3  loadc R3 \_fac
i = 4  move R4 R1   x-1
i = 5  loadc R5 1
i = 6  sub R4 R4 R5
i = 5  move R\_1 R4  fac(x-1)
i = 3  saveloc R1 R2
mark
call R3
restoreloc R1 R2
move R3 R0
\_B:  return
r
\end{verbatim}