Programming Languages

Concurrency: Memory Consistency

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Thread A

```c
void foo(void) {
    a = 1;
    b = 1;
}
```

Thread B

```c
void bar(void) {
    while (b == 0) {};
    assert (a == 1);
}
```

**Intuition**: the assertion will never fail

⚠️ **Real execution**: given enough tries, the assertion may eventually fail

~~> in need of defining a *Memory Model*
Memory Models

Memory interactions behave differently in presence of
- multiple concurrent threads
- data replication in hierarchical and/or distributed memory systems
- deferred communication of updates

Memory Models are a product of negotiating
- restrictions of freedom of implementation to guarantee race related properties
- establishment of freedom of implementation to enable *program* and *machine model* optimizations

Modern Languages include the memory model in their language definition
Motivated by sequential computing, we intuitively implicitly transfer our idea of semantics of memory accesses to concurrent computation. This leads to our idealistic model *Strict Consistency*:

**Definition (Strict consistency)**

Independently of which process reads or writes, the value from the most recent write to a location is observable by reads from the respective location immediately after the write occurs.

Although idealistically desired, practically not existing

⚠️ absolute global time problematic

⚠️ physically not possible

⇝ strict consistency is too strong to be realistic
Abandoning absolute time

Thread A

```c
void foo(void) {
    a = 1;
    b = 1;
}
```

Thread B

```c
void bar(void) {
    while (b == 0) {}
    assert(a == 1);
}
```

- initial state of `a` and `b` is 0
- `A` writes `a` before it writes `b`
- `B` should see `b` go to 1 before executing the `assert` statement
- the `assert` statement should always hold

⇝ here correctness means: writing a 1 to `a` happens before reading a 1 in `b`

Still, *any* of the following may happen:

⇝ Idea: state correctness in terms of what event *may* happen before another one
Happend-Before Relation and Diagram
Events in a Distributed System

A process as a series of events [Lam78]: Given a distributed system of processes $P, Q, R, \ldots$, each process $P$ consists of events $\bullet p_1, \bullet p_2, \ldots$.

Example:

- event $\bullet p_i$ in process $P$ happened before $\bullet p_{i+1}$
- if $\bullet p_i$ is an event that sends a message to $Q$ then there is some event $\bullet q_j$ in $Q$ that receives this message and $\bullet p_i$ happened before $\bullet q_j$
The Happened-Before Relation

Definition

If an event $p$ happened before an event $q$ then $p \rightarrow q$.

Observe:

- $\rightarrow$ is partial (neither $p \rightarrow q$ or $q \rightarrow p$ may hold)
- $\rightarrow$ is irreflexive ($p \rightarrow p$ never holds)
- $\rightarrow$ is transitive ($p \rightarrow q \land q \rightarrow r$ then $p \rightarrow r$)
- $\rightarrow$ is asymmetric (if $p \rightarrow q$ then $\neg(q \rightarrow p)$)

$\Rightarrow$ the $\rightarrow$ relation is a strict partial order
Concurrent in Happened-Before Diagrams

Let $a \nleftrightarrow b$ abbreviate $\neg(a \rightarrow b)$.

**Definition**

Two distinct events $p$ and $q$ are said to be **concurrent** if $p \nleftrightarrow q$ and $q \nleftrightarrow p$.

$p_3 \nrightarrow q_3$ and $q_3 \nrightarrow p_3$ in the example.

$p_3$ and $q_3$ are, in fact, concurrent since $p_3 \nleftrightarrow q_3$ and $q_3 \nleftrightarrow p_3$.
Ordering

Let $C$ be a logical clock i.e. $C$ assigns a globally unique time-stamp $C(p)$ to each event $p$.

Definition (Clock Condition)

Function $C$ satisfies the clock condition if for any events $p, q$

$$p \rightarrow q \quad \Rightarrow \quad C(p) < C(q)$$

For a distributed system the clock condition holds iff:

1. $p_i$ and $p_j$ are events of $P$ and $p_i \rightarrow p_j$ then $C(p_i) < C(p_j)$
2. $p$ is the sending of a message by process $P$ and $q$ is the reception of this message by process $Q$ then $C(p) < C(q)$

→ a logical clock $C$ that satisfies the clock condition describes a total order $a < b$ (with $C(a) < C(b)$) that embeds the strict partial order $\rightarrow$

The set defined by all $C$ that satisfy the clock condition is exactly the set of executions possible in the system.

→ use the process model and $\rightarrow$ to define better consistency model
Defining $C$ Satisfying the Clock Condition

Given:

\[\begin{array}{c}
P \quad p_1 \quad p_2 \quad p_3 \quad p_4 \\
Q \quad q_1 \quad q_2 \quad q_3 \quad q_4 \quad q_5 \quad q_6 \quad q_7 \\
R \quad r_1 \quad r_2 \quad r_3 \quad r_4 \\
\end{array}\]

<table>
<thead>
<tr>
<th>$e$</th>
<th>$p_1$</th>
<th>$p_2$</th>
<th>$p_3$</th>
<th>$p_4$</th>
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<tr>
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<td>11</td>
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<tr>
<td>$C(e)$</td>
<td>8</td>
<td>9</td>
<td>10</td>
<td>15</td>
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</table>
Summing up Happened-Before Relations

We can model concurrency using processes and events:

- there is a *happened-before* relation between the events of each process
- there is a *happened-before* relation between communicating events
- *happened-before* is a strict partial order
- a clock is a total strict order that embeds the *happened-before* partial order
Memory Consistency Models based on the Happened-Before Relation
Happened-Before Based Memory Models

Idea: use happened-before diagrams to model more relaxed memory models.

Given a path through each of the threads of a program:
- consider the actions of each thread as events of a process
- use more processes to model memory
  - here: one process per variable in memory
- ⇝ concisely represent some interleavings

⇝ We establish a model for Sequential Consistency.
Sequential Consistency

**Definition (Sequential Consistency Condition [Lam78])**

The result of any execution is the same as if the memory operations
- of each individual processor appear in the order specified by its program
- of all processors joined were executed in some sequential order

### Sequential Consistency applied to Multiprocessor Programs:

Given a program with $n$ threads,

1. for fixed event sequences $p_0^1, p_1^1, \ldots$ and $p_0^2, p_1^2, \ldots$ and $p_0^n, p_1^n, \ldots$ keeping the program order,

2. executions obeying the clock condition on the $p_i^j$,

3. all executions have the same result

Yet, in other words:

- 1. defines the *execution path* of each thread
- each execution mentioned in 2 is one *interleaving* of processes
- 3. declares that the result of running the threads with these interleavings is always the same.
Sequential Consistency in Multiprocessor Programs:

Given a program with \( n \) threads,

1. for fixed event sequences \( p_0^1, p_1^1, \ldots \) and \( p_0^2, p_1^2, \ldots \) and \( p_0^n, p_1^n, \ldots \) keeping the program order,
2. executions obeying the clock condition on the \( p_j^i \),
3. all executions have the same result

Idea for showing that a system is not sequentially consistent:

- pick a result obtained from a program run on a SC system
- pick an execution \( \mathbf{1} \) and a total ordering of all operations \( \mathbf{2} \)
- add extra processes to model other system components
- the original order \( \mathbf{2} \) becomes a partial order \( \rightarrow \)
- show that total orderings \( C' \) exist for \( \rightarrow \) for which the result differs
Weakening the Model

**Observation:** more concurrency possible, if we model each memory location separately, i.e. as a different process

Sequential consistency still obeyed:
- the accesses of `foo` to `a` occurs before `b`
- the first two read accesses to `b` are in parallel to `a=1`

**Conclusion:** There is no observable change if accesses to different memory locations can happen in parallel.
Benefits of Sequential Consistency

- concisely represent all interleavings that are due to variations in timing
- synchronization using time is uncommon for software
- a good model for correct behaviors of concurrent programs
- program results besides SC results are undesirable (they contain races)

Realistic model for simple hardware architectures:

- sequential consistency model suitable for concurrent processors that acquire exclusive access to memory
- processors can speed up computation by using caches and still made to maintain sequential consistency

Not realistic for elaborate hardware with out-of-order stores:

- what other processors see is determined by complex optimizations to cacheline management

⇝ internal workings of caches
Introducing Caches: The MESI Protocol
The MESI Protocol: States [PP84]

Processors use caches to avoid a costly round-trip to RAM for every memory access.
- programs often access the same memory area repeatedly (e.g. stack)
- keeping a local mirror image of certain memory regions requires bookkeeping about who has the latest copy

Each cache line is in one of the states $M, E, S, I$:
- $I$: it is *invalid* and is ready for re-use
- $S$: other caches have an identical copy of this cache line, it is *shared*
- $E$: the content is in no other cache; it is *exclusive* to this cache and can be overwritten without consulting other caches
- $M$: the content is exclusive to this cache and has furthermore been *modified*

⇝ the global state of cache lines is kept consistent by sending *messages*
The MESI Protocol: Messages

Moving data between caches is coordinated by sending messages [McK10]:

- **Read**: sent if CPU needs to read from an address
- **Read Response**: when in state E or S, response to a Read message, carries the data for the requested address
- **Invalidate**: asks others to evict a cache line
- **Invalidate Acknowledge**: reply indicating that a cache line has been evicted
- **Read Invalidate**: like Read + Invalidate (also called “read with intend to modify”)
- **Writeback**: Read Response when in state M, as a side effect noticing main memory about modifications to the cacheline, changing sender’s state to S

We mostly consider messages between processors. Upon Read Invalidate, a processor replies with Read Response/Writeback before the Invalidate Acknowledge is sent.
MESI Example

Consider how the following code might execute:

### Thread A

```plaintext
a = 1;  // A.1
b = 1;  // A.2
```

### Thread B

```plaintext
while (b == 0) {}; // B.1
assert(a == 1);   // B.2
```

- In all examples, the initial values of variables are assumed to be 0.
- Suppose that `a` and `b` reside in different cache lines.
- Assume that a cache line is larger than the variable itself.
- We write the content of a cache line as:
  - `Mx`: modified, with value `x`
  - `Ex`: exclusive, with value `x`
  - `Sh`: shared, with value `x`
  - `I`: invalid
Thread A

\[a = 1; \quad \text{// A.1}\]
\[b = 1; \quad \text{// A.2}\]

Thread B

\[
\textbf{while} \ (b == 0) \ \{} \ \}; \quad \text{// B.1}
\]
\[\text{assert}(a == 1); \quad \text{// B.2}\]

<table>
<thead>
<tr>
<th>statement</th>
<th>CPU A</th>
<th>CPU B</th>
<th>RAM</th>
<th>message</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>a</td>
<td>b</td>
<td>a</td>
<td>b</td>
</tr>
<tr>
<td>A.1</td>
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<td>0</td>
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<td>M1</td>
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</table>

**read invalidate** of \(a\) from CPU A
**invalidate ack.** of \(a\) from CPU B
**read response** of \(a=0\) from RAM

**read** of \(b\) from CPU B
**read response** with \(b=0\) from RAM

**read invalidate** of \(b\) from CPU A
**read response** of \(b=0\) from CPU B
**invalidate ack.** of \(b\) from CPU B
Thread A

\[
\begin{align*}
a &= 1; & \quad & \text{// A.1} \\
b &= 1; & \quad & \text{// A.2}
\end{align*}
\]

Thread B

\[
\begin{align*}
\text{while } (b == 0) \{} & \\
\text{assert } (a == 1); & \quad & \text{// B.2}
\end{align*}
\]

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<td>(a)</td>
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<td>(a)</td>
<td>(b)</td>
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<td>B.2</td>
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MESI Example: Happened Before Model

Idea: each cache line one process, A caches $b=0$ as E, B caches $a=0$ as E

Observations:
- each memory access must complete before executing next instruction ⇔ add edge
- second execution of test $b==0$ stays within cache ⇔ no traffic
Sequential consistency:

- a characterization of well-behaved programs
- a model for differing speed of execution
- for fixed paths through the threads and a total order between accesses to the same variable: executions can be illustrated by happened-before diagram with one process per variable
- MESI cache coherence protocol ensures SC for processors with caches
Introducing Store Buffers: Out-Of-Order Stores
Out-of-Order Execution

⚠️ performance problem: writes always stall

### Thread A

\[
\begin{align*}
a &= 1; & \text{ // A.1} \\
b &= 1; & \text{ // A.2}
\end{align*}
\]

### Thread B

\[
\begin{align*}
\text{while } (b == 0) & \{ \\ & \text{ // B.1} \\
\text{assert } (a == 1) & ; & \text{ // B.2}
\end{align*}
\]

⇝ CPU A should continue executing after \( a=1; \)
Store Buffers and Total Store Ordering [SI92]

**Goal:** continue execution after *cache-miss* write operation

- put each write into a *store buffer* and trigger fetching of cache line
- once a cache line has arrived, apply relevant writes
  - today, a store buffer is always a *queue* [OSS09]
  - two writes to the same location are not merged
- sequential consistency per *CPU* is violated unless
  - each read checks store buffer before cache
  - on hit, return the youngest value that is waiting to be written
  \[\rightsquigarrow TSO\]

**Excursion**: non-FIFO store buffers

\[\rightsquigarrow Sparc/PSO\]
Definition (Total Store Order)

1. The store order wrt. memory (⊆) is total

\[ \forall a,b \in \text{addr}, i,j \in \text{CPU} \quad (\text{St}_i[a] \subseteq \text{St}_j[b]) \lor (\text{St}_j[b] \subseteq \text{St}_i[a]) \]

2. Stores in program order (≤) are embedded into the memory order (⊆)

\[ \text{St}_i[a] \leq \text{St}_i[b] \Rightarrow \text{St}_i[a] \subseteq \text{St}_i[b] \]

3. Loads preceding an other operation (wrt. program order ≤) are embedded into the memory order (⊆)

\[ \text{Ld}_i[a] \leq \text{Op}_i[b] \Rightarrow \text{Ld}_i[a] \subseteq \text{Op}_i[b] \]

4. A load's value is determined by the latest write as observed by the local CPU

\[ \text{val}(\text{Ld}_i[a]) = \text{val}(\text{St}_j[a] \mid \text{St}_j[a] = \max (\{\text{St}_k[a] \mid \text{St}_k[a] \subseteq \text{Ld}_i[a]\} \cup \{\text{St}_i[a] \mid \text{St}_i[a] \leq \text{Ld}_i[a]\})) \]

Particularly, one ordering property is not guaranteed:

\[ \text{St}_i[a] \leq \text{Ld}_i[b] \not\Rightarrow \text{St}_i[a] \subseteq \text{Ld}_i[b] \]

⚠️ Local stores may be observed earlier by local loads then from somewhere else!

What about sequential consistency for the whole system?
Happened-Before Model for Store Buffers

Thread A

\[
a = 1; \\
b = 1;
\]

Thread B

\[
\text{while } (b == 0) \{ \} ; \\
\text{assert}(a == 1);
\]

Assume cache A contains: a: S0, b: E0, cache B contains: a: S0, b: I
Explicit Synchronization: Write Barrier

Overtaking of messages *is desirable* and should not be prohibited in general.

- store buffers render programs incorrect that assume sequential consistency between *different* CPUs
- whenever two stores in one CPU must appear *in sequence at a different CPU*, an explicit *write barrier* has to be inserted
  - a write barrier marks all current store operations in the store buffer
  - the next store operation is only executed when all marked stores in the buffer have completed
- x86 CPUs provide the *sfence* instruction
- a write barrier after each write gives sequentially consistent CPU behavior (and is as slow as a CPU without store buffer)

⇝ use (write) barriers only when necessary
Happened-Before Model for Write Barriers

Thread A

\[ a = 1; \]
\[ \text{sfence}(); \]
\[ b = 1; \]

Thread B

\[ \text{while} (b == 0) \{ \}; \]
\[ \text{assert}(a == 1); \]

Assume cache A contains: a: S0, b: E0, cache B contains: a: S0, b: I
Introducing Invalidate Queues: O-o-O Reads
Invalidate Queue

Invalidation of cache lines is costly:
- all CPUs in the system need to send an acknowledge
- invalidating a cache line competes with CPU accesses
- a cache-intense computation can fill up store buffers in other CPUs

立即承认一个无效化并稍后再应用
- 放入每个无效化消息到一个无效化队列
  - 如果一个MESI消息需要被发送关于在无效化队列中的一个缓存行，则等到线被无效化
- ![本地读写不咨询无效化队列](image)

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What about sequential consistency?
Happened-Before Model for Invalidate Queues

**Thread A**

a = 1;
sfence();
b = 1;

**Thread B**

while (b == 0) {};
assert (a == 1);

Assume cache A contains: a: S0, b: E0, cache B contains: a: S0, b: l
Explicit Synchronization: Read Barriers

Read accesses do not consult the invalidate queue.
- might read an out-of-date value
- need a way to establish sequential consistency between writes of other processors and local reads
- insert an explicit read barrier before the read access
  - a read barrier marks all entries in the invalidate queue
  - the next read operation is only executed once all marked invalidations have completed
- Intel x86 CPUs provide the lfence instruction
- a read barrier before each read gives sequentially consistent read behavior (and is as slow as a system without invalidate queue)

match each write barrier in one process with a read barrier in another process
Happened-Before Model for Read Barriers

Thread A

\[ a = 1; \]
\[ \text{sfence}(); \]
\[ b = 1; \]

Thread B

\[ \text{while} \ (b == 0) \ \{ \}; \]
\[ \text{lfuscene}(); \]
\[ \text{assert}(a == 1); \]
Example: The Dekker Algorithm on SMP Systems
Using Memory Barriers: the Dekker Algorithm

Mutual exclusion of two processes with busy waiting.

//flag[] is boolean array; and turn is an integer
flag[0] = false;
flag[1] = false;
turn = 0; // or 1

P0:
flag[0] = true;
while (flag[1] == true) {
    if (turn != 0) {
        flag[0] = false;
        while (turn != 0) {
            // busy wait
        }
    }
    flag[0] = true;
}
// critical section
turn = 1;
flag[0] = false;

P1:
flag[1] = true;
while (flag[0] == true) {
    if (turn != 1) {
        flag[1] = false;
        while (turn != 1) {
            // busy wait
        }
    }
    flag[1] = true;
}
// critical section
turn = 0;
flag[1] = false;
The Idea Behind Dekker

Communication via three variables:

- \( \text{flag}[i]==\text{true} \) process \( P_i \) wants to enter its critical section
- \( \text{turn}==i \) process \( P_i \) has priority when both want to enter

\[P0:\]
flag[0] = true;
while (flag[1] == true)
  if (turn != 0) {
    flag[0] = false;
    while (turn != 0) {
      // busy wait
    }
    flag[0] = true;
  }
// critical section
turn = 1;
flag[0] = false;

In process \( P_i \):

- if \( P_{1-i} \) does not want to enter, proceed immediately to the critical section
- \( \Rightarrow \) flag[i] is a lock and may be implemented as such
- if \( P_{1-i} \) also wants to enter, wait for turn to be set to \( i \)
- while waiting for turn, reset flag[i] to enable \( P_{1-i} \) to progress
Dekker’s Algorithm and TSO

Problem: Dekker’s algorithm requires sequential consistency.
Idea: insert memory barriers between all variables common to both threads.

P0:
flag[0] = true;
sfence();
while (lfence(), flag[1] == true) {
  if (lfence(), turn != 0) {
    flag[0] = false;
sfence();
    while (lfence(), turn != 0) {
      // busy wait
    }
    flag[0] = true;
sfence();
  }
// critical section
turn = 1;
sfence();
flag[0] = false; sfence();

- insert a load memory barrier `lfence()` in front of every read from common variables
- insert a write memory barrier `sfence()` after writing a variable that is read in the other thread
- the `lfence()` of the first iteration of each loop may be combined with the preceding `sfence()` to an `mfence()`
Highly optimized CPUs may use an even more relaxed memory model:
- reads and writes are not synchronized unless requested by the user
- many kinds of memory barriers exist with subtle differences
  ⇝ ARM, PowerPC, Alpha, ia-64, even x86 (⇝ SSE Write Combining)

- This is interesting to pursue, but there is so much else to cover...

⇝ memory barriers are the “lowest-level” of synchronization
Discussion

Memory barriers reside at the lowest level of synchronization primitives. Where are they useful?

- when blocking should not de-schedule threads
- when several processes implement automata and coordinate their transitions via common synchronized variables
- protocol implementations
- OS provides synchronization facilities based on memory barriers

Why might they not be appropriate?

- difficult to get right, best suited for specific well-understood algorithms
- often synchronization with locks is as fast and easier
- too many fences are costly if store/invalidate buffers are bottleneck

What do compilers do about barriers?

- C/C++: it’s up to the programmer, use `volatile` for all thread-common variables to avoid optimizations which are only correct for sequential programs
- Java: the JVM inserts barriers automatically for `volatile` variables
Memory Models and Compilers

Before Optimization

```c
x = 0;
for (int i=0; i<100; i++) {  
x = 1;
    printf("%d", x);
}
```

After Optimization

```c
x = 1;
for (int i=0; i<100; i++) {  
    printf("%d", x);
}
```

Standard Program Optimizations

comprises *loop-invariant code motion* and *dead store elimination*, e.g.

⚠️ having another thread executing `x = 0;` changes observable behaviour depending on optimizing or not

✠ Compiler also depends on consistency guarantees
✠ Demand for Memory Models on language level
Summary

Learning Outcomes

1. Strict Consistency
2. Happened-before Relation
3. Sequential Consistency
4. The MESI Cache Model
5. TSO: store/invalidate buffers
6. Reestablishing Sequential Consistency with memory barriers
7. Dekker’s Algorithm for Mutual Exclusion
Many-Core Machines’ Read Responses congest the bus

In that case: Intel’s *MESIF* (Forward) to reduce communication overhead.

⚠️ But in general, Symmetric multi-processing (SMP) has its limits:

- a memory-intensive computation may cause contention on the bus
- the speed of the bus is limited since the electrical signal has to travel to all participants
- point-to-point connections are faster than a bus, but do not provide possibility of forming consensus

⇝ use a bus locally, use point-to-point links globally: *NUMA*

- *non-uniform memory access* partitions the memory amongst CPUs
- a directory states which CPU holds a memory region
- Interprocess communication between Cache-Controllers (*ccNUMA*): onchip on Opteron or in chipset on Itanium
Overhead of NUMA Systems

Communication overhead in a NUMA system.

- Processors in a NUMA system may be fully or partially connected.
- The directory of who stores an address is partitioned amongst processors.

A cache miss that cannot be satisfied by the local memory at A:

- A sends a retrieve request to processor B owning the directory
- B tells the processor C who holds the content
- C sends data (or status) to A and sends acknowledge to B
- B completes transmission by an acknowledge to A

source: [Int09]
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